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10/749,571	12/31/2003	Mikko Waltari	88537.0067	8970

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EXAMINER	
WAMSLEY, PATRICK G	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 04/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,571	WALTARI, MIKKO	
	Examiner	Art Unit	
	Patrick G. Wamsley	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/22/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the parallel operation of the ADC processing unit and the sample-and-hold, hereafter S/H, circuit must be shown or canceled from the claim 1. Moreover, no drawings show how the S/H circuit is "integrated" with the MDAC, as recited in claims 3 and 26, or how a single operational amplifier is used for multiple operations, as recited in claims 1, 15, and 24. While Figure 4 depicts an ADC processing unit [102 / 104: Page 9, ¶40], it does not show a sample-and-hold circuit. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 9 and 18 are objected to because of the following informalities:

Claim 9, line 3: Change "switched coupled" to -- coupled --.

Claim 9, line 4: Change "capacitor are" to -- capacitors are --.

Claim 18, line 3: Change "applied to switched" to -- applied to the switched --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-13, 15, 17-22, 24, and 26-28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. On line 4 of claim 1, applicant declares that the ADC processing unit and the sample-and-hold, hereafter S/H, circuit both share a single operational amplifier and operate in parallel. While this limitation appears in the specification [Page 4, ¶06], it is not described in sufficient detail to enable the invention.

Applicant admits that known algorithmic ADCs comprise at least two single-bit processing units sharing a common operational amplifier [Page 3, ¶4]. However, no details are provided, so the examiner cannot compare this admission properly with the use of a single operational amplifier asserted in claims 1, 15, and 24. Moreover, it is unclear how the invention is analogous to the process used in conventional pipelined ADCs [Page 8, ¶38].

Applicant declares that this invention has a heavily serial operation principle [Page 8, ¶36]. If so, how can the basic units of the device be placed in a parallel configuration and still follow a heavily serial pattern? Does the term "parallel" only refer to internal blocks, such as the sub-ADC [104: Page 10, ¶45]?

How is the S/H circuit simultaneously both "parallel" to the MDAC and integrated with it? U.S. Patent 5,952,952 to Choi shows a switched-capacitor array used in stages of pipelined ADCs, as depicted in Figure 6. The illustrated stage includes both a S/H circuit [240] and a DAC [220]. However, Choi indicates that all element enclosed within the dotted lines [box 200] may be replaced by a single MDAC [col. 5, lines 47-51]. As best understood by the examiner, this operation "integrates" a MDAC with a S/H circuit. However, a rejection will not be made at this time in order to give applicant time to further explain the meaning of claims 1-13, 15, 24, and 26-28.

Regarding claims 17-22, applicant recites an "intermediate analog voltage" on line 7 of claim 17. How does this voltage differ from the residue? While residue generation is disclosed in the specification, it is unclear what is meant by an intermediate analog voltage in claim 17. Is it a new residue voltage replacing a previous residue voltage? A new sample voltage? See ¶41 on Page 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 14, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art, hereafter APA, in view of U.S. Patent 5,952,952 to Choi et al, hereafter Choi.

APA discloses an algorithmic analog-to-digital converter [Page 2, ¶3], hereafter ADC, able to sample a continuous analog signal and quantize it into a set of discrete levels. Thus, APA discloses both a S/H function [sampling], and an ADC operation [quantization]. APA's algorithmic ADCs also comprise at least two single-bit processing units sharing a common operational amplifier [Page 3, ¶4].
Unlike claim 14, APA has two MDAC units [Page 20, ¶76] instead of one.

In contrast, Choi uses a single MDAC unit [col. 5, lines 47-51] in a pipelined stage of an ADC. At the time of the invention, it would have been obvious to one of ordinary skill in the art to have applied Choi's teachings to APA's ADC. The motivation would have been to reduce chip surface area [col. 2, line 63].

Claims 23 and 25, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art, hereafter APA, in view of U.S. Patent 5,847,600 to Brooks et al, hereafter Brooks.

As mentioned above, APA provides S / H and ADC functions. Conventional algorithmic ADCs [Page 20, ¶76] have two MDACs operating in opposite phases - one generates a residue, while the other performs sampling. These MDACs inherently comprise switched capacitor circuits, which were also described as "typical" by applicant on page 9, ¶40. Such circuits inherently have feedback signals in the context of an ADC system, as the DAC itself serves as a feedback element. As best understood, the invention differs from APA by generating multiple bits in a single pipeline stage.

Brooks provides a pipelined ADC that converts multiple bits in its first stage [abstract, lines 7-8]. The first stage flash ADC [214] provides a n-bit digital word [col. 1, lines 30-31], having five bits or more [col. 8, line 23].

For claim 25, applicant admits that the operation of a full flash ADC is well known to those of skill in the art [Page 18, ¶69]. Moreover, Brooks uses a flash ADC to provide multiple bits in a single stage. Thus, the APA / Brooks combination appear to satisfy the claim, generating multiple bits with a flash ADC stage.

Allowable Subject Matter

Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the references of record neither reveal nor render obvious generation of five sets of bits per sample-and-hold clock period. While Brooks generates five bits in a first stage, they are not arranged into set of bits.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 6,822,601 to Liu et al discloses a pipelined ADC having a MDAC stage. U.S. Patent 6,636,084 to Sarraj provides a S/H circuit including an operational amplifier [12] and a plurality of switched capacitors. U.S. Patent 6,563,348 to Beck et al uses a single operational amplifier [203] for double-sampling a signal. U.S. Patent 6,541,952 to Nagaraj couples S/H subcircuits in parallel.

U.S. Patent 6,326,818 to Sculley provides a S/H circuit with a switched capacitor integrator [120]. U.S. Patent 6,285,309 to Yu shows a nested pipelined ADC having five bit stages [col. 5, line 58]. U.S. Patent 6,127,958 to Chang et al discloses an ADC having a MDAC [202] coupled to a sub-ADC [206]. U.S. Patent 4,529,965 to Lee describes an algorithmic technique for a switched-capacitor ADC.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick G. Wamsley whose telephone number is (571) 272-1814. The official facsimile number is (703) 872-9306. An alternate facsimile number, (571) 273-1814, should only be used for unofficial documents.

Patrick G. Wamsley
April 8, 2005